Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-16. (Canceled)

17. (New) A manufacturing method of a semiconductor device including at least two MISFETs, one of which is a P-type MISFET and the other of which is an N-type MISFET, the method comprising:

forming a buried insulating film in a semiconductor substrate;

forming MISFETs isolated by the buried insulating film;

cleaning a surface side of the semiconductor substrate with a cleaning solution; and

covering a surface side of the buried insulating film with a protective film before cleaning the surface side of the semiconductor substrate, wherein the protective film is resistant to the cleaning solution.

18. (New) The manufacturing method of the semiconductor device according to claim 17, wherein the cleaning solution is a hydrofluoric acid based solution.

19. (New) The manufacturing method of the semiconductor device according to claim 18, wherein the hydrofluoric acid based solution is a hydrogen fluoride (HF) solution or an ammonium fluoride (NH_4F) solution.

20. (New) The manufacturing method of the semiconductor device according to claim 18, wherein the protective film is a material which is resistant to the hydrofluoric acid based solution.

21. (New) The manufacturing method of the semiconductor device according to claim 20, wherein the protective film is a silicon nitride film.

22. (New) The manufacturing method of the semiconductor device according to claim 21, the manufacturing method further comprising forming a sidewall on a side portion of a gate electrode of the MISFET, and

wherein the sidewall and the protective film are the same material.

23. (New) The manufacturing method of the semiconductor device according to claim 22, further comprising forming a salicide metal layer on the gate electrode, a source diffusion region, and a drain diffusion region of the MISFET after the step of cleaning the surface side of the semiconductor substrate.

24. (New) The manufacturing method of the semiconductor device according to claim 17, wherein the protective film is formed so as to cover a portion of a diffusion region of the P-type MISFET and a portion of a diffusion region of the N-type MISFET.

25. (New) The manufacturing method of the semiconductor device according to claim 24, further comprising forming a wiring layer which is formed on the protective film and which electrically connects the diffusion region of the P-type MISFET and the diffusion region of the N-type MISFET.